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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,129	02/28/2002	David P. Schultz	X-1069 US	2232

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,129	SCHULTZ, DAVID P.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communicati n appears on th cov r sh et with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Office Action in response to AMENDMENT filed 9/30/2004, in reply to the Office Action mailed 6/28/2004.

Claims 1-27 are pending and presently under examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 and 6–27 are rejected under 35 U.S.C. 102(e) as being anticipated by Nadeau-Dostie et al. (US 6829730), ISSUED: December 7, 2004, FILED: April 27, 2001.

Regarding independent Claim 1, Nadeau-Dostie discloses a method for design of integrated circuits having multiple Test Access Port (TAP) interfaces, for flexibly nesting JTAG TAP controllers (14, 16) for IP cores (18, 20), Figures 1-3, the method comprising:

Selecting via multiplexer (132) at least one available bit (five bits), from a selectable bit register (instruction register 125) of the Master TAP 100 controller, the selectable bit register (125) having a plurality of available bits (eight bits), Figure 3.

Extending an apparent length of an instruction register (116) from the initial three shift register elements to a total of (eight bits) by using the five selected bits from the selectable register 125.

Regarding independent Claim 7, Nadeau-Dostie discloses a method for design of integrated circuits having multiple Test Access Port (TAP) interfaces, for flexibly nesting JTAG TAP controllers (14, 16) for IP cores (18, 20), Figures 1-3, the method comprising:

Choosing at least one IP core JTAG TAP controller (102) from a plurality of JTAG TAP controllers (TAPS 102, 104 and 106), using a selection code for selecting via multiplexer 130 the TAP controller (102) of group 112, Figure 3. The controllers (TAPS 102, 104 and 106) are also illustrated in Figure 1, which are nested in cores (18, 20) corresponding to TAP controllers (14, 16).

Programmable connecting the selected IP core JTAG TAP controller (102,) to a host JTAG TAP controller (Master TAP 100), Figure 3. Also, Figure 1 shows a typical arrangement of TAPs of Figure 3 contained in a circuit 10, having a first Master TAP 12, which generates control signals for two embedded TAP 14 and TAP 16.

Selecting an apparent length of an instruction register (116) from the initial three shift register elements to a total of (eight bits) by using the five selected bits from the

selectable register 125, based upon a number of IP cores (18, 20) implemented in the circuit 10.

Regarding independent Claim 11, Nadeau-Dostie discloses a system for design of integrated circuits having multiple Test Access Port (TAP) interfaces, for flexibly accessing nested JTAG TAP controllers (14, 16) for IP cores (18, 20), Figures 1-3, the system comprising:

A selectable bit register (instruction register 125) of the Master TAP 100 controller, the selectable bit register (125) having a plurality of available bits (eight bits), Figure 3.

A selector multiplexer (132) for selecting (five bits) from the selectable bit register (instruction register 125), the selector 132 extending an apparent length of an instruction register (116) from the initial three shift register elements to a total of (eight bits) by using the five selected bits from the selectable register 125, Figure 3.

Regarding independent Claim 14, Nadeau-Dostie discloses a system for design of integrated circuits having multiple Test Access Port (TAP) interfaces, for flexibly accessing nested JTAG TAP controllers (14, 16) for IP cores (18, 20), Figures 1-3, the system comprising:

A selection code for selecting TAP controller (102) of group 112, via multiplexer 130, from a plurality of JTAG TAP controllers (TAPS 102, 104 and 106). The controllers

(TAPS 102, 104 and 106) are also illustrated in Figure 1, which are nested in cores (18, 20) corresponding to TAP controllers (14, 16).

A multiplexer 132 for programmably connecting the selected IP core JTAG TAP controller (102,) to a host JTAG TAP controller (Master TAP 100), Figure 3. Also, Figure 1 shows a typical arrangement of TAPs of Figure 3 contained in a circuit 10, having a first Master TAP 12, which generates control signals for two embedded TAP 14 and TAP 16 controllers.

An instruction register size select signal (Shift-IR) for controlling Multiplexer 132 and 134 to determine the source of the data loaded into a TAP group. When an instruction is loaded into an instruction register, Shift-IR is active (Logic 1), which connect input 1 of each of multiplexer 132 and 134 to their respective group TDI input. The (Shift-IR) signal enables the selection via Multiplex 132 of the apparent length of the instruction register (116) from the initial three shift register elements to a total of (eight bits) by using the five selected bits from the selectable register 125, for the purpose of accommodating TAP controllers (14, 16) for IP cores (18, 20), shown in Figures 1 and 3.

Regarding independent Claim 18, Nadeau-Dostie discloses a method for design of integrated circuits having multiple Test Access Port (TAP) interfaces, for flexibly nesting JTAG TAP controllers (14, 16) for IP cores (18, 20), Figures 1-3, the method comprising:

Forming instruction registers 116, 118 and 120 corresponding to three embedded TAPS 102, 104 and 106, shown by dotted rectangles for the IP cores, which are serially connected with the instruction register 125 and each instruction register group (112 and 114) forming an eight bit extended size, by selecting available bits from 125 via multiplexer 132 and 134.

Forming connections between JTAG TAP (14, 16) Core Logic and IP Core (18 and 20), using a programmable interconnect.

Emulating instruction registers (116, 118 and 120) of the IP core (18, 20), each having (eight bit) length, which is the same length as the instruction register 125.

Regarding independent Claim 21, Nadeau-Dostie discloses a system for design of integrated circuits having multiple Test Access Port (TAP) interfaces, for performing boundary scan functions on a plurality of IP cores (18, 20), Figure 1, the system comprising:

An FPGA-based system-on-chip (SoC) Figure 1 showing a typical arrangement of TAPs contained in a circuit 10, comprising a plurality of IP cores (18, 20) each including a JTAG TAP controller (eTAP1 14 and eTAP2 16),

A host JTAG TAP controller (TAP 12, Master TAP) coupled to each of the JTAG TAP controllers 14 and 16, the host JTAG TAP controller 12 comprising a selectable bit register 125 for selecting an apparent length of an instruction register (116) from the initial three shift register elements to a total of (eight bits) by using the five selected bits

from the selectable register 125, based upon a number of IP cores (18, 20) implemented in the circuit 10.

Regarding Claims 2, 12, Nadeau-Dostie discloses a selection code for selecting via multiplexer 130 the TAP controller (102) of group 112, from a plurality of JTAG TAP controllers (TAPS 102, 104 and 106). The controllers (TAPS 102, 104 and 106) are also illustrated in Figure 1, which are nested in cores (18, 20) corresponding to TAP controllers (14, 16), and communicably accessible by the host JTAG TAP controller (TAP 12, Master TAP, Figure 1) or as shown as (Master TAP 100 controller, Figure 3).

Regarding Claim 3, Nadeau-Dostie discloses extending is done to emulate an instruction register (102) of an IP core 18 before configuration of an FPGA on the SoC (10), Figure 1 and 3.

Regarding Claims 4, 10, 13, 17, Nadeau-Dostie discloses shifting an instruction using (Shift-IR) for the chosen IP core JTAG TAP controller (102) through the instruction register 116 having the extended length, causing thee IP core JTAG TAP controller (102) to execute the instruction.

Regarding Claim 6, Nadeau-Dostie discloses programmably selecting the available bit (five bits) from the selectable bit register 125, via Multiplexer 132, using select signal (Shift-IR).

Regarding Claim 8, Nadeau-Dostie discloses selecting via multiplexer (132) at least one available bit (five bits), from a selectable bit register (instruction register 125)

of the Master TAP 100 controller, the selectable bit register (125) having a plurality of available bits (eight bits), Figure 3.

Regarding Claim 9, Nadeau-Dostie discloses extending an apparent length of an instruction register (116) from the initial three shift register elements to a total of (eight bits) by using the five selected bits from the selectable register 125.

Regarding Claim 15, Nadeau-Dostie discloses a selectable bit register 125 for host JTAG TAP (Master TAP 100) controller, the selectable bit register (125) having a plurality of available bits (eight bits), Figure 3.

Regarding Claim 16, selectable bit register 125 extending an apparent length of an instruction register (116) from the initial three shift register elements to a total of (eight bits) by using the five selected bits from the selectable register 125, comprising the instruction register.

Regarding Claim 19, Nadeau-Dostie discloses accessing the nested JTAG TAP controllers (TAPS 102, 104 and 106) of the IP cores (18, 20) via a programmable Input / output (via multiplexer 130) using a selection code, Figure 3.

Regarding Claim 20, extending is done to emulate an instruction register (102) of an IP core 18 based on configuration of an FPGA on the SoC (10), Figure 1 and 3.

Regarding Claim 22, Nadeau-Dostie discloses FPGA on the SoC (10), including host JTAG TAP 12, shown in Figure 1, and also shown as a (Master TAP 100), in Figure 3.

Regarding Claims 23, 26, Nadeau-Dostie discloses a selector circuit (multiplexer 130, Figure 3) coupled between TAP 12, called Master TAP and two embedded

(secondary) TAPs, called eTAP1 14 and eTAP2 16. Note: multiplexer 130 is part of TAP 12 of Figure 1.

Regarding Claims 24, 27, the FPGA-based SOC (10) includes the host JTAG TAP controller 12 and the selector circuit (multiplexer 130, Figure 3).

Regarding Claim 25, Nadeau-Dostie discloses selectable bit register 125 comprising an input terminal TDI coupled to the selector circuit 130 and an output terminal TDO providing a selected bit, wherein the host JTAG TAP controller 100 comprising an instruction register (116) having an apparent length extended from the initial three shift register elements to a total of (eight bits) by using the five selected bits from the selectable register 125, as shown in Figure 3.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. (US 6829730).

Regarding Claim 5, Nadeau-Dostie discloses the claimed invention as applied to claim 1 above. Nadeau-Dostie does not explicitly disclose manually selecting available

bits from the selectable bit register. However, Nadeau-Dostie discloses a Multiplexer 132, using select signal (Shift-IR) for selecting the available bit (five bits) from the selectable bit register 125, upon programmable (Shift-IR) command. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a manual select command in the Multiplexer 132 of Nadeau-Dostie, by logically performing an "OR" function between programmable (Shift-IR) command or manual command, since Nadeau-Dostie provides the hardware and software for such design modification.

Response to Arguments

Applicant's arguments, see remarks of AMENDMENT filed 9/30/2004, with respect to the rejection of claims 1-27 under 35 U.S.C. 102(e) as being anticipated by Haroun et al. (US 6324662), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Claims 1-4 and 6–27 rejected under 35 U.S.C. 102(e) as being anticipated by Nadeau-Dostie et al. (US 6829730), and Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. (US 6829730), as set forth in the present Office Action.

Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
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Date: 7 January 2005
Office Action: Non-Final Rejection

By: _____

JAMES C KERVEROS
Examiner
Art Unit 2133

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